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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,960	MILLER ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005 and 18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *58-65,68-72 and 75-120* is/are pending in the application, wherein claims 1-57, 66-67, 73-74 are cancelled.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *78-120* is/are allowed.

6)☒ Claim(s) *58-65,68-72 and 75-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner and by the draftsperson.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 3/14/2005, arguments and Application Data Sheet filed on 2/18/2005. Claims 58-65,68-72,75-120 are pending, wherein claims 1-57,66-67,73-74 are cancelled and claims 58,60-61,65,71,81,88,100,111,118 have been amended. Claims 58-65,68-72,75-120 have been examined, wherein claims 78-120 are allowed, as previously indicated, and claims 58-65,68-72,75-77 are newly rejected as being necessitated by Applicant's amendment to the claims.

Priority

2. Acknowledgement is made of the Application Data Sheet filed on 2/18/2005, which properly referenced the domestic claimed priority document to U.S. Application No. 09/437,996, which is a non-provisional of the provisional U.S. Patent Application No. 60/159,687. Accordingly, the claimed priority in the Oath and Declaration has been corrected.

Drawings

3. The drawings were received on 2/18/2005. These drawings are approved by the Examiner and by the draftsperson.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the

applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 58-65,68,71-72,75-76** are rejected under 35 U.S.C. 102(e) as being anticipated by **Hill** (US Patent No. 6,370,673).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per **claim 58**, Fig. 3 illustrates the elements of the claims, wherein the netlist(s) is/are received at step 225 (i.e., technology independent netlist received by technology dependent synthesis process) and step 235 (i.e., technology dependent netlist received by design rule checking process), wherein such netlist(s) is/are further described in col. 6, lines 37-58; col. 7, lines 6-14; wherein the coarse placement corresponds to step 255 (see col. 7, lines 15-35 coarse placement with floating point coordinates cell assignment); wherein the detailed placement corresponds to step 260 (see col. 7, lines 37-51 for detailed placement with snapping (i.e., aligning) cell from its floating point coordinates to a nearest legal location); wherein the synthesis process corresponds to steps 215 and 225; wherein the specification of the placement area is

received at step 255 as part of the constraints or objectives as described in col. 7, 20-25 which are usually part of the specification (see also col. 1, lines 38-46) and received step 260, as a result from the coarse placement step 250 (see col. 7, lines 15-50; col. 8, lines 23-57).

As per **claims 59-60**, all of the elements of claim 58, from which the claim depends, are discussed in the rejection of claim 58 above, wherein the detail placement process being limited to only performing legalization such that the cells are assigned to legal sites without violating constraints set forth in the specification of the placement area is also described in col. 7, lines 37-50 (i.e., placement into legal positions, which includes alignment or snapping of cells, eliminating overlaps).

As per **claim 61**, all of the elements of claims 59, from which the claim depends, are discussed in the rejection of claim 59 above, wherein the detailed placement process including defining a master objective function to evaluate a goodness of a cell placement corresponds to the lowest cost function used in step 330 (Fig. 4A) since it is used to evaluate the goodness or best of cell placement.

As per **claim 62**, all of the elements of claims 58, from which the claim depends, are discussed in the rejection of claim 58 above, wherein the iterating the detailed placement process is illustrated in Fig. 4A, loops 325, 340, 345, and the iteration of the synthesis process is illustrated in Fig. 3, loops 225, 230, 235, 240.

As per **claim 63**, all of the elements of claim 58, from which the claim depends, are discussed in the rejection of claim 58 above, wherein since the synthesis process

includes modeling timing estimation, such timing driven synthesis process is also within the scope of **Hill** (see col. 6, lines 45-57).

As per **claim 64**, all of the elements of claim 58, from which the claim depends, are discussed in the rejection of claim 58 above, wherein the coarse placement process is a congestion driven is also part of the optimization objective for at least wire routability (col. 7, lines 20-25).

As per **claim 65**, Fig. 3 illustrates the elements of the claims, wherein the detailed placement corresponds to step 260 (see col. 7, lines 37-51 for detailed placement with snapping (i.e., aligning) cell from its floating point coordinates to a nearest legal location); wherein the synthesis process corresponds to steps 215 and 225; wherein the iteration of the detailed placement process is illustrated in Fig. 4A, loops 325, 340, 345 until the conditions are met (i.e., convergence--until all cells are optimally placed), and the iteration of the synthesis process is illustrated in Fig. 3, loops 225, 230, 235, 240 until the conditions are met (i.e., convergence--until there are no design rules violation).

As per **claim 68**, all of the elements of claims 65 from which the claim depends, are discussed in the rejection of claim 65 above, wherein the further elements of the claims are also discussed in the rejection of claim 63 above.

As per **claim 71**, Fig. 3 illustrates the elements of the claims, wherein the detailed placement corresponds to step 260 (see col. 7, lines 37-51 for detailed placement with snapping (i.e., aligning) cell from its floating point coordinates to a nearest legal location); wherein the synthesis process corresponds to steps 215 and

225 wherein since the synthesis process includes modeling timing estimation, such timing driven synthesis process is also within the scope of **Hill** (see col. 6, lines 45-57); wherein the detailed placement process and the synthesis process are integrated in the sense they are performed together in the same CAD environment.

As per **claim 72**, all of the elements of claim 71, from which the claim depends, are discussed in the rejection of claim 71 above, wherein the detailed placement process only performs legalization is also described in col. 7, lines 37-50 (i.e., placement into legal positions, which includes alignment or snapping of cells, eliminating overlaps).

As per **claim 75**, all of the elements of claim 71, from which the claim depends, are discussed in the rejection of claim 71 above, wherein the iteration of the detailed placement process is illustrated in Fig. 4A, loops 325, 340, 345 until the conditions are met (i.e., convergence--until all cells are optimally placed), and the iteration of the synthesis process is illustrated in Fig. 3, loops 225, 230, 235, 240 until the conditions are met (i.e., convergence--until there are no design rules violation).

As per **claim 76**, all of the elements of claim 71, from which the claim depends, are discussed in the rejection of claim 71 above, wherein the congestion driven placement is also part of the coarse placement in which the optimization objective is for at least wire routability (col. 7, lines 20-25).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 58-65,68-72,76-77** are rejected under 35 U.S.C. 103(a) as being obvious over **Eng** (US Patent Application Publication No. 2002/0059553) in view of **Hill** (US Patent No. 6,370,673).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claim 58**, **Eng** discloses the elements of the claims are illustrated in Fig. 2, wherein the netlist is received at least from blocks 202 and 228 as the results of the logic or LBB synthesis (202, 228), the specification for placement is received at least from blocks 223-226, 222, 216, 214, 205, wherein the initial placement is performed in at least blocks 215, 213 (see also paragraphs [0187]), the detailed placement is performed in blocks 227,229,231 (see also paragraphs [0188]-[0189]), and the synthesis process is performed in blocks 202,228. However, **Eng** fails to teach the use of floating point coordinates for cell locations as part of the coarse placement process and the snapping of cells from the floating point coordinates to a nearest legal location as part of the detailed placement process. **Hill** teaches coarse placement using floating point coordinates and detailed placement involving snapping of cells from floating point coordinates to a nearest legal location, so that the cells can be initially be placed precisely without worry about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal locations (col. 7, lines 15-35; col. 1, lines 47-64; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention incorporate the use of floating point coordinates and the snapping of cells as taught by **Hill** into the method/system of **Eng** because such use of floating point coordinates and the snapping of cells would further allow the method/system of **Eng** to provide initial cells placement to be precisely placed without worrying about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal locations, as taught by **Hill**, while benefiting

from the method/system of RTL optimization prior to conventional logic synthesis, floorplanning, and place-and-route design stages, of **Eng** (paragraphs [0015]-[0016]).

As per **claim 59-60**, **Eng** in view of **Hill** teaches all of the elements of claim 58, from which the claims depend, as discussed previously, wherein the detailed placement process performing only legalization (i.e., moving cells to legal or non-overlapping sites) is also taught by **Eng** as part of the compaction step 1303 described in paragraph [0188] and also taught by **Hill** (col. 7, lines 37-50).

As per **claims 61**, **Eng** in view of **Hill** teaches all of the elements of claim 59, from which the claim depends, as discussed previously, wherein the movement of a minimum distance (i.e., minimum perturbance) to achieve legalization (i.e., non-overlapping) is further taught in **Eng** (paragraph [0265]).

As per **claim 62**, **Eng** in view of **Hill** teaches all of the elements of claim 58, from which the claim depends, as discussed previously, wherein **Eng** further teaches the iteration of the detailed placement process and synthesis process as illustrated in the design flow shown in Fig. 2, wherein the synthesis (228) is iterated via the chip optimizer 213 through the paths of blocks 229, 231, 232, 218, 213 (see also paragraph [0008]).

As per **claim 63, Eng** in view of **Hill** teaches all of the elements of claim 58, from which the claim depends, as discussed previously, wherein **Eng** further teaches the synthesis being timing driven as described in paragraph [0038].

As per **claims 64**, **Eng** in view of **Hill** teaches all of the elements of claim 58, from which the claim depends, as discussed previously, wherein **Eng** further teaches

the coarse placement being congestion driven as described in [0187] as part of the force-directed method and iteratively improved by packing the clusters, which inherently eliminates or reduce congestion, as is well known in the art, allowing the feasible implementations.

As per **claim 65**, **Eng** teaches the detailed placement process performing only legalization (i.e., snapping or moving cells to legal or non-overlapping sites) is part of the compaction step 1303 described in paragraph [0188], wherein the synthesis (block 228) and detailed placement (blocks 227,229,231) being performed several times is illustrated in Fig. 2. However, **Eng** failed to teach the snapping of the cell from floating point coordinates to a nearest legal location as part of the detailed placement process. **Hill** teaches coarse placement using floating point coordinates and detailed placement involving snapping of cells from floating point coordinates to a nearest legal location, so that the cells can be initially be placed precisely without worry about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal locations (col. 7, lines 15-35; col. 1, lines 47-64; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention incorporate the use of floating point coordinates and the snapping of cells as taught by **Hill** into the method/system of **Eng** because such use of floating point coordinates and the snapping of cells would further allow the method/system of **Eng** to provide initial cells placement to be precisely placed without worrying about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal

locations, as taught by **Hill**, while benefiting from the method/system of RTL optimization prior to conventional logic synthesis, floorplanning, and place-and-route design stages, of **Eng** (paragraphs [0015]-[0016]).

As per **claim 68, Eng** in view of **Hill** teaches all of the elements of claim 65, from which the claim depends, as discussed previously, wherein **Eng** further teaches the synthesis being timing driven as described in paragraph [0038].

As per **claim 69**, **Eng** in view of **Hill** teaches all of the elements of claim 65, from which the claim depends, as discussed previously, wherein **Eng** further teaches the coarse placement being performed before the detailed placement and synthesis process as also illustrated in Fig. 2, wherein at least initial placements blocks 210 and 212 are performed prior to the synthesis 228 and detailed placement blocks 227,229,231.

As per **claim 70**, **Eng** in view of **Hill** teaches all of the elements of claim 69, from which the claim depends, as discussed previously, wherein **Eng** further teaches the coarse (initial) placement with minimized wire length as described in paragraph [0187]. **Hill** also teaches these further limitations (see col. 7, lines 15-35).

As per **claim 71-72,75**, **Eng** teaches the detailed placement including only performing legalization and synthesis, the iteration thereof, as discussed in the rejection of claim 65 above, wherein the synthesis being timing driven is described in paragraph [0038], and wherein the integration of the detailed placement and synthesis is illustrated in Fig. 2, being integrated as part of the chip optimizer 213. However, **Eng** fails to teach the snapping of cell to its nearest legal site. **Hill** teaches the use of

snapping of cells to its nearest legal location as part of the detailed placement process, so that the cells can be initially be placed precisely without worry about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal locations (col. 7, lines 15-35; col. 1, lines 47-64; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention incorporate the use snapping of cells as taught by **Hill** into the method/system of **Eng** because such snapping of cells would further allow the method/system of **Eng** to provide initial cells placement to be precisely placed without worrying about the actual grid alignment and then during a detailed placement process, be later aligned with proper matrix of allowable x and y discrete grids for legal locations, as taught by **Hill**, while benefiting from the method/system of RTL optimization prior to conventional logic synthesis, floorplanning, and place-and-route design stages, of **Eng** (paragraphs [0015]-[0016]).

As per **claim 76**, **Eng** in view of **Hill** teaches all of the elements of claim 71, from which the claim depends, as discussed previously, wherein **Eng** further teaches the coarse placement being congestion driven as described in [0187] as part of the force-directed method and iteratively improved by packing the clusters, which inherently eliminates or reduce congestion, as is well known in the art, allowing the feasible implementations.

As per **claim 77**, **Eng** in view of **Hill** teaches all of the elements of claim 71, from which the claim depends, as discussed previously, wherein **Eng** further teaches the

coarse (initial) placement with minimized wire length as described in paragraph [0187]. **Hill** also teaches these further limitations (see col. 7, lines 15-35).

8. **Claims 71-72,75-77** are rejected under 35 U.S.C. 102(e) as being anticipated by **Eng** (US Patent Application Publication No. 2002/0059553) in view of **Ding** (US Patent No. 5,801,959).

As per **claim 71-72,75**, **Eng** discloses the detailed placement including only performing legalization (i.e., as part of the compaction step 1303 described in paragraph [0188]), and synthesis, wherein the synthesis (block 228) and detailed placement (blocks 227,229,231) being performed several times is illustrated in Fig. 2.; wherein the synthesis being timing driven is described in paragraph [0038], and wherein the integration of the detailed placement and synthesis is illustrated in Fig. 2, being integrated as part of the chip optimizer 213. However, **Eng** fails to teach the cell being snapped to its nearest legal site as part of the detailed placement process as claimed. **Ding** teaches the routing and placement in which the cell(s) are being snapped to the nearest legal location on the routing or placement grid, reducing the number of iterations required to produced an optimal placement (col. 12, line 32 to col. 13, line 13; col. 2, lines 22-32; col. 3, lines 1-19). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the snapping method of **Ding** into the routing/placement of **Eng** because such incorporation would further results in less time (i.e., the number of iterations are reduced) while providing optimal placement.

As per **claim 76**, **Eng** in view of **Ding** disclose all of the elements of claim 71 above, which the claim depends are discussed in the rejection of claim 76 above; wherein **Eng** further discloses the coarse placement being congestion driven as described in [0187] as part of the force-directed method and iteratively improved by packing the clusters, which inherently eliminates or reduce congestion, as is well known in the art, allowing the feasible implementations.

As per **claim 77**, **Eng** in view of **Ding** disclose all of the elements of claim 71 above, from which the claim depends, as discussed in the rejection of claim 71 above, wherein **Eng** further discloses the coarse (initial) placement with minimized wire length as described in paragraph [0187].

Allowable Subject Matter

9. **Claims 78-120** are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 78-120**, Applicant's preliminary amendment and arguments filed on 5/1/2003 set forth the patentability of Applicant's claimed invention, wherein as pointed out by Applicant, the independent claims 78,90,102,114-121, which the optimized cost function dependent on the sites in pairs of rows, are used as part of the detailed placement process and the swapping of cells between pairs of rows, as part of the method for placing cells of a netlist, as claimed, which the prior arts made of record failed to teach or suggest (see preliminary amendment filed on 5/1/2003, pages 16-18).

Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Remarks

11. The objections of **claims 66,67,81,88,89,100,111,118** are withdrawn in light Applicant's amendment filed on 3/14/2005, which corrected claims 81,88,89,100,118,118, and muted the objections of claims 66-67 since the claims are cancelled.

12. The rejections of **claims 58-65,68-72,75-77** under 35 U.S.C. 102(e) as being anticipated by **Eng** (US Patent Application Publication No. 2002/0059553) are withdrawn in light of Applicant's amendment filed on 3/14/2005, wherein as pointed out by Applicant, **Eng** fails to teach the new limitations as amended by Applicant, including use of floating point coordinates for cell locations as part of the coarse placement process, the use of snapping a cell from its floating point coordinates to a nearest legal location as part of the step of performing a detailed placement process, and/or the use of snapping a cell to its nearest legal site, as claimed. However, as given in the new rejections above, being necessitated by Applicant's amendment to the claims, claims 58-65,68,71-72,75-76 are not patentable over **Hill** (US Patent No. 6,370,673); claims 58-65,68-72,76-77 are not patentable over **Eng** (US Patent Application Publication No. 2002/0059553) in view of **Hill** (US Patent No. 6,370,673); and claims 71-72,75-77 are not patentable over **Eng** (US Patent Application Publication No. 2002/0059553) in view of **Ding** (US Patent No. 5,801,954); wherein the new limitations are taught by **Hill**

and/or **Ding** alone or in combination with **Eng** as given above, for the reasons given above.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents
P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(571) 273-1895 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

PK
June 21, 2005

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800